

Fig. 1

Incoming Data

Phase Detector

Fig. 2

Clock

State of the art

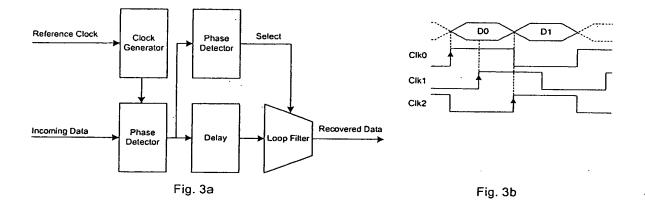
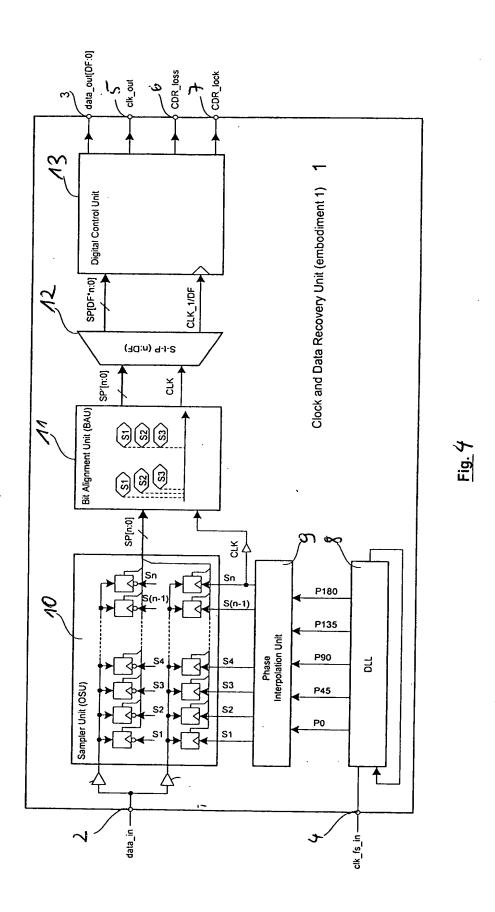
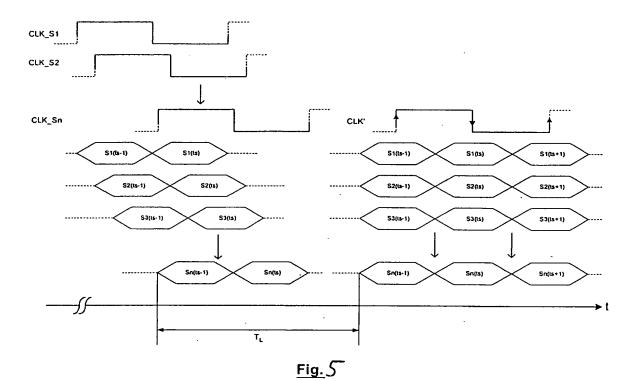
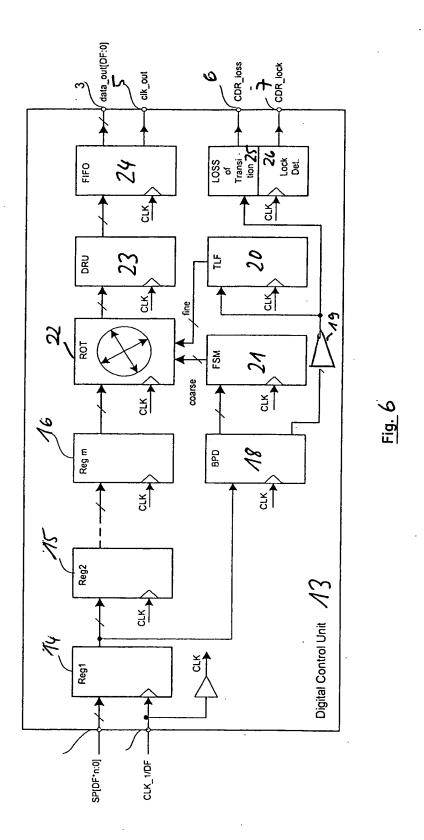


Fig. 3







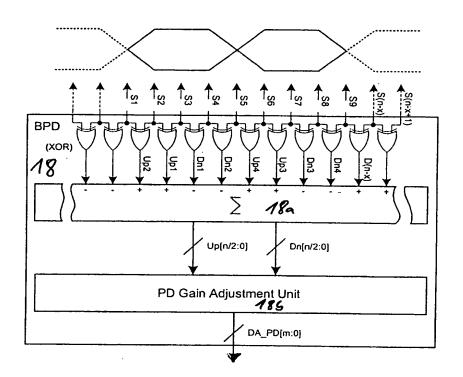
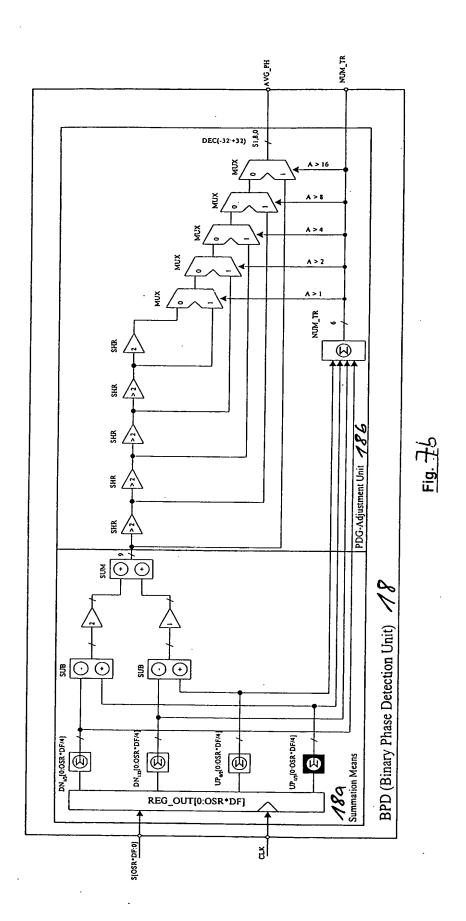
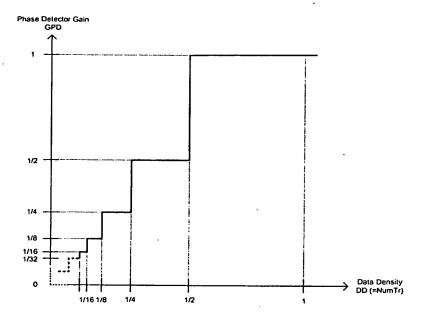


Fig. 7a





State of the art

Fig. 8a

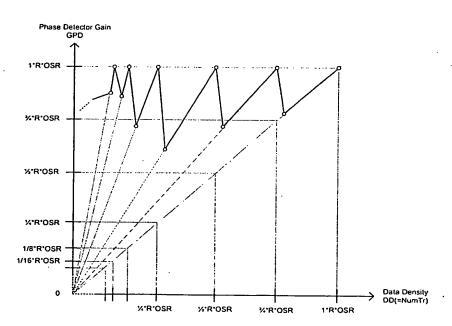


Fig. 8b

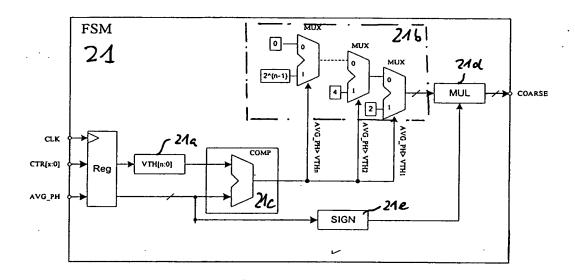


Fig. 9

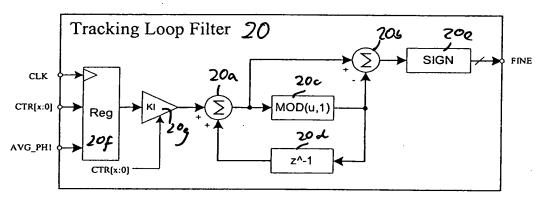
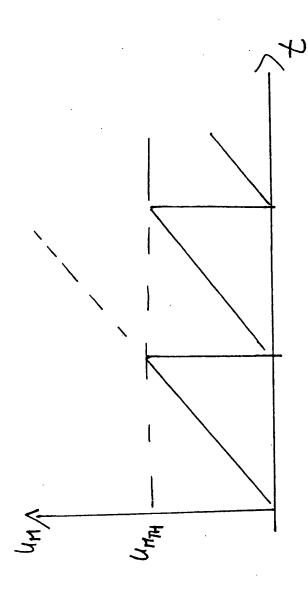


Fig. 10





Title: A FEED FORWARD CLOCK AND DATA RECOVERY UNIT

Applicant: Peter Gregorius Atty Docket: 1406/145/2

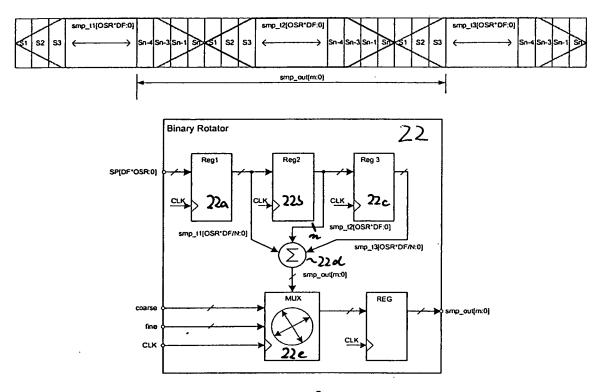


Fig. 12_

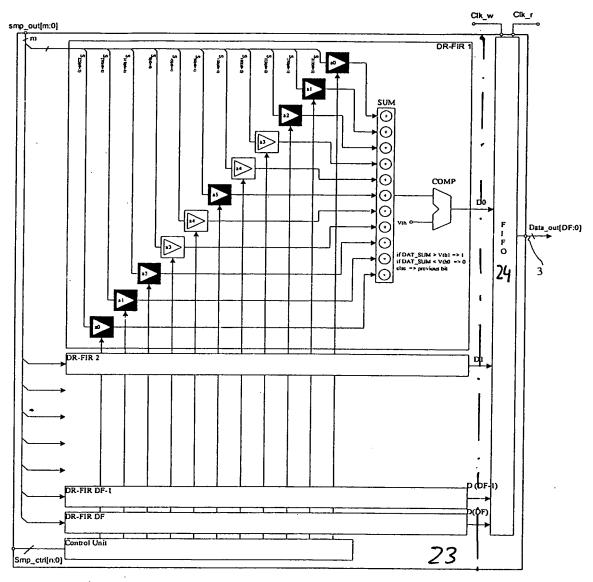
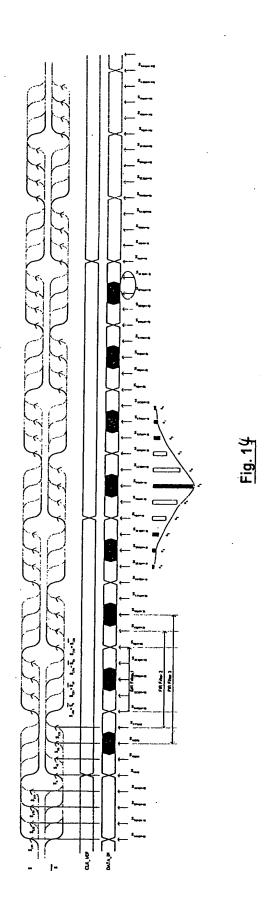
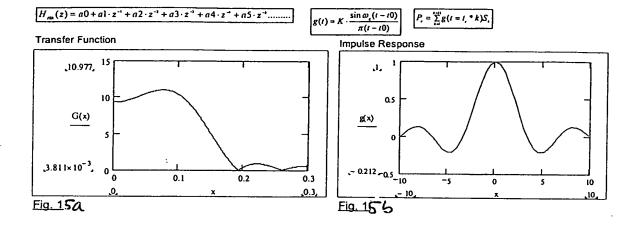


Fig. 13



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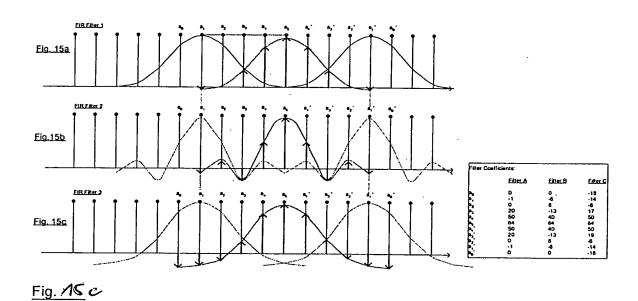


Fig. 15

